AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings of claims in the application:

LISTING OF CLAIMS:

1-12 (canceled)

13. (currently amended) A component with a logic circuit arrangement with configurable functionality, comprising a plurality of data lines (7), at least a portion of the data lines (7) being assigned at least one element (1) that can be switched between two states with different discrete resistances, by means of which element (1) the data line (7) is enabled or inhibited depending on the switched state, it being possible for the switching state of the element (1) to be stored in nonvolatile fashion and to be changed over rapidly, characterized in that wherein i) the element is connected to a gate of a pass transistor (8), the pass transistor is connected into the data line (7) and is inhibited or enabled by means of the element (1), or ii) the element (1) itself is used as a pass transistor that enables or inhibits the data line (7), with the element (1) connected directly into the data line and directly opening or inhibiting the latter, or iii) the element is connected in parallel with the data line and short-circuits the latter or behaves in transparent fashion in that the element (1) itself is

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used as the pass transistor that enables or inhibits the data line (7).

- 14. (currently amended) The component as claimed in claim 13, characterized in that wherein the element (1) is an element exhibiting a magnetoresistive effect.
- 15. (currently amended) The component as claimed in claim 14, characterized in that wherein the element (1) is a TMR cell (2).
- 16. (currently amended) The component as claimed in claim 13, characterized in that wherein the element (1) exhibits a resistance change as a result of a phase change generated during switching, in particular from an amorphous state to a crystalline state.
- 17. (currently amended) The component as claimed in claim 16, characterized in that wherein the element (1) is an OUM cell.
- 18. (currently amended) The component as claimed in claim 13, a pass transistor (8) connected into the data line (7) being inhibited or enabled by means of the element (1), characterized in that wherein only one element (1) or two

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elements (1) coupled to one another and operated in parallel is/are provided for actuating the pass transistor (8).

- 19. (currently amended) The component as claimed in claim 18, characterized in that wherein two TMR cells (2) are provided, which are driven in inverted fashion.
- 20. (currently amended) The component as claimed in claim 19, characterized in that wherein the two elements (1), in particular the are two TMR cells (2), have having a resistance ratio between the two state-related resistances not equal to 1:1, in particular of 1:2 or more.
 - 21. (cancelled).
- 22. (currently amended) The component as claimed in claim [[21]] 13, characterized in that wherein the element (1) is one of a, in particular the TMR cell (2) or the and a OUM cell, has/have the element having a resistance ratio between the two state-related resistances of at least 1:5, in particular of at least 1:10 or greater.

- 23. (currently amended) The component as claimed in claim 13, characterized in that wherein the switching time for changing over the resistance of the element is $\leq 5 \, \mathrm{ns}$, in particular $\leq 3 \, \mathrm{ns}$.
- 24. (new) A component with a logic circuit arrangement with configurable functionality, comprising:

a plurality of data lines (7);

at least a portion of the data lines (7) being assigned an element (1) that can be switched between two states with different discrete resistances, by means of which element (1) the data lines (7) are enabled or inhibited depending on the switched state of the element (1),

wherein the switching state of the element (1) is stored in nonvolatile fashion,

wherein i) a pass transistor (8) connected into the data lines (7) is inhibited or enabled by means of the element (1), or ii) the element (1) itself is configured as the pass transistor that enables or inhibits the data lines (7), and

wherein the element (1) exhibits a resistance change as a result of a phase change generated during switching from an amorphous state to a crystalline state.

25. (new) The component as claimed in claim 24, wherein the element (1) is an OUM cell.

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26. (new) A component with a logic circuit arrangement with configurable functionality, comprising:

a plurality of data lines (7);

at least a portion of the data lines (7) being assigned two elements (1) that can be switched between two states with different discrete resistances, by means of which two elements (1) the data lines (7) are enabled or inhibited depending on the switched state of the element (1),

wherein the switching state of the two elements (1) is stored in nonvolatile fashion,

wherein a pass transistor (8) connected into the data lines (7) is inhibited or enabled by means of the two elements (1),

wherein the two elements (1) are coupled to one another and operated in parallel, and

wherein the two elements are two TMR cells (2) driven in inverted fashion.

- 27. (new) The component as claimed in claim 26, wherein the two TMR cells (2) have a resistance ratio between the two state-related resistances not equal to 1:1.
- 28. (new) The component as claimed in claim 24, the element (1) itself being used as the pass transistor that enables

or inhibits the data line (7), wherein the element (1) is connected directly into the data line and directly opens or inhibits the latter, or in that the element is connected in parallel with the data line and short-circuits the latter or behaves in transparent fashion.

- 29. (new) The component as claimed in claim 28, wherein the element (1) has a resistance ratio between the two state-related resistances of at least 1:5.
- 30. (new) The component as claimed in claim 24, characterized in that the switching time for changing over the resistance of the element is $\leq 5 \, \mathrm{ns}$.
- 31. (new) The component as claimed in claim 24, characterized in that the switching time for changing over the resistance of the element is $\leq 3 \text{ns}$.